

Enrollment No: _____ Exam Seat No: _____

C.U.SHAH UNIVERSITY

Summer Examination-2017

Subject Name: Language Processor Designing

Subject Code: 5TE02LPD1

Branch: M.Tech (CE)

Semester: 2

Date: 06/05/2017

Time: 02:00 To 05:00

Marks: 70

Instructions:

- (1) Use of Programmable calculator and any other electronic instrument is prohibited.
 - (2) Instructions written on main answer book are strictly to be obeyed.
 - (3) Draw neat diagrams and figures (if necessary) at right places.
 - (4) Assume suitable data if needed.
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SECTION – I

Q-1 Attempt the Following questions (07)

- a. Define: Predictive Parser.
- b. Define: Cross-Compiler.
- c. Define: Macros.
- d. List various types of Editors.
- e. Define: Deterministic Automata.
- f. Define : Context Free Grammar
- g. What is Lex and YACC?

Q-2 Attempt all questions (14)

- a. Explain Two Pass assemblers.
- b. What is Symbol Table? Explain

OR

Q-2 Attempt all questions (14)

- a. Explain Relocation Process.
- b. Explain Various Loading Types.

Q-3 Attempt all questions (14)

- a. Describe the lexical, syntactic and semantic phases of compiler.
- b. What is Error in compiler? Explain various error recovery strategies of parser

OR

Q-3 Attempt all questions (14)

- a. What are the major points of differences between Interpreter and Compiler?
- b. Construct NFA for following regular expression and convert it into DFA

$a^+ b^* (c | d | e) a^* \#$



SECTION – II

Q-4 Attempt the Following questions (07)

- a. Define: Lexemes.
- b. Define: Loader.
- c. Define: Parsing.
- d. Define: Peephole Optimization.
- e. Justify Role of Lexical Analyzer.
- f. What is DAG?
- g. What is Ambiguity in grammar?

Q-5 Attempt all questions (14)

- a. What is Activation Record? Explain
- b. Explain macro expansion

OR

Q-5 Attempt all questions (14)

- a. Explain different kind of Procedure calls.
- b. How to optimize code in compiling process? Explain the process.

Q-6 Attempt all questions (14)

- a. Check whether the given grammar is LL (1) or not.

$E \rightarrow T'$
 $E \rightarrow TE' \mid \varepsilon$
 $T \rightarrow VT'$
 $T' \rightarrow /VT' \mid \varepsilon$
 $V \rightarrow \langle id \rangle$

- b. Explain overlays with suitable example.

OR

Q-6 Attempt all Questions (14)

- a. Explain various storage allocation strategies
- b. Describe Design issues in code generator.

